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Determination of Intrinsic FET Parameters Using Circuit Partitioning Approach

Hans-Olof Vickes

Abstract—**A technique useful in extracting intrinsic parameters for a compound semiconductor FET is presented. The technique makes use of a method provided by Dambrine *et al.* [8]. A modified active circuit that accounts for charge accumulation in the conducting channel is presented. The model has the further advantage of using control voltage modeling in agreement with the Curtice convention for large-signal analysis. The equations are presented for each active element as a function of the intrinsic *y* parameters. Measurements verify the parameter extraction technique with the circuit topology used and show good results.**

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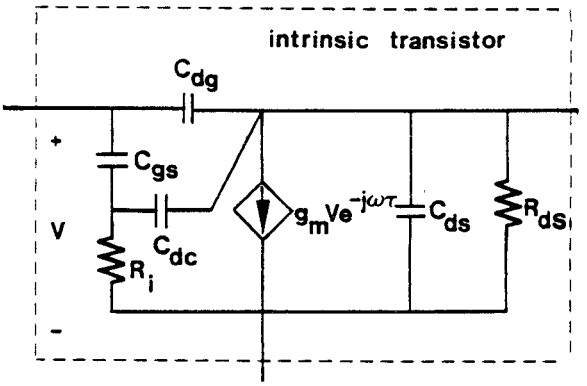

Fig. 1. Active FET model with control voltage modeled over the total $C_{gs}-R_i$ combination (after Curtice [10]). The current source is modeled with a linear transconductance, g_m, and an associated transit time delay, τ.

I. INTRODUCTION

A physically based small-signal equivalent circuit of a field-effect transistor is very useful in the development of new circuit design guidelines for both microwave and digital GaAs integrated circuits. Such a model is usually obtained by optimizing the component values to closely fit the small-signal microwave scattering parameters for the device in question. However, this circuit parameter determination technique is old-fashioned and is not advisable because it has several drawbacks:

i) The unduly large number of variables for the optimization algorithm (likelihood of stopping at a local minimum).
ii) Several resulting element values become dependent upon optimization.

Thus, using this technique we can obtain a physically invalid circuit [1].

To overcome these difficulties appropriate decomposition schemes should be considered. Important contributions with special relevance to microwave decomposition can be found in [2]–[8]. The method developed by Dambrine *et al.* [8] seems to be the most powerful measurement technique yet described.

The objective of this paper is to exploit the above method of extraction of the intrinsic *y* parameters for a better understanding of the high-frequency performance of compound semiconductor FET's. Thus, by using simple matrix manipulations, the intrinsic matrix is determined. Here we further develop and refine the intrinsic FET description. In addition, we use a symmetrical T network to model the coplanar waveguide with lower ground plane (CPWG) at the input and output terminals of the device in question. In this manner, we can show how an accurate FET equivalent circuit topology is used to generate high-frequency equivalent circuits for compound semiconductor FET's.

II. ANALYSIS

The measurement technique of the extrinsic elements constitutes a key point in the paper by Dambrine *et al.* [8] and is clearly explained. Therefore, in this paper we focus on the intrinsic FET description. To examine the small-signal intrinsic *y* parameters of compound semiconductor FET's, we use the

TABLE I
CPWG MODELED AS A SYMMETRICAL T NETWORK

	Physical Layout Parameters (μm) $H = 625$			Equivalent Circuit Components (nH, pF)				Relative
$\epsilon_r = 13$	W	G	L	L_G	C_G	L_D	C_D	Error
Input	60	60	50	0.02446	0.00876			10^{-5}
Output	20	80	80			0.05724	0.00876	$3.2 \cdot 10^{-7}$

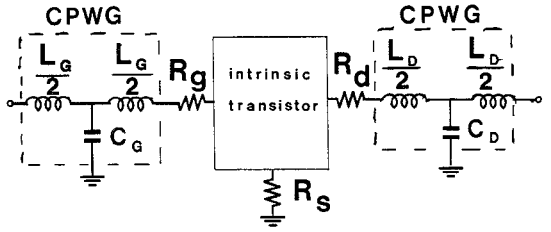

Fig. 2. Complete equivalent circuit with coplanar transmission lines at input and output.

matrix manipulation scheme of their paper. These parameters were extracted from S-parameter data after removal of parasitics through a method of successive z-to-y and y-to-z transformations.

The intrinsic part of a FET is shown in Fig. 1. The intrinsic device may be characterized by the y parameters, namely,

$$y_{11} = j\omega C_{gs}\frac{1+j\omega\tau_1}{1+j\omega\tau_2} + j\omega C_{dg} \tag{1}$$

$$y_{12} = -j\omega C_{dg} + \frac{\omega^2 C_{gs}\tau_1}{1+j\omega\tau_2} \tag{2}$$

$$y_{21} = g_m e^{-j\omega\tau} + y_{12} \tag{3}$$

$$y_{22} = \frac{1}{R_{ds}} + j\omega\left(C_{ds} + C_{dg} + C_{dc}\right) + \frac{\omega^2\tau_1 C_{dc}}{1+j\omega\tau_2} \tag{4}$$

where

$$\tau_1 = R_i C_{dc}$$
$$\tau_2 = R_i\left(C_{gs} + C_{dc}\right).$$

Notice that the active FET model in Fig. 1 differs from the model used by [8]. Here we added a capacitance, C_{dc}, and changed the drain–source current to be controlled by the voltage across C_{gs} and R_i, not just C_{gs} alone. This change in the small-signal circuit can be justified by the following:

i) The internal feedback capacitance, C_{dc}, physically results from a nonuniform free charge density in the conducting channel for both GaAs MESFET's [9] and MODFET's. In addition, C_{dc} causes the reverse transfer conductance (i.e., $\mathrm{Re}(y_{12})$) to have a positive sign and a square-law frequency dependence. This improves modeled data to more closely fit experimental S_{12} data at higher frequencies.
ii) Modeling of the control voltage across C_{gs} and R_i is the convention used by Curtice in large-signal modeling. This forces the time delay factor, τ, to account for all delay effects under the gate and permits the value of R_i to be based upon input loss [10].

The concept of an equivalent circuit representation is an abstraction and a simplification of a physical device. It provides, however, a way to describe the electrical behavior of the circuit in a proper way. At the same time it is important to keep the complexity of the equations on a level that is manageable. Once the equivalent circuit is decided upon, no additional simplification should be introduced. It has been shown in [12] and [14] how low-frequency approximations can result in erroneous results for high-frequency applications.

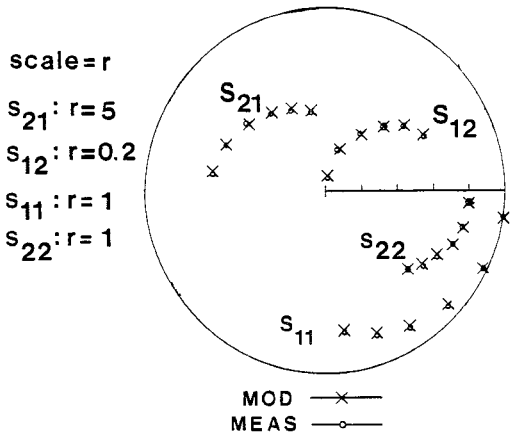

Fig. 3. Smith chart display of two-port S parameters of a MODFET with a mushroom gate 0.25 μm. Frequency start at $f = 2$ GHz and sampled every 4 GHz up to 22 GHz. × simulations; ○ measurements.

III. PARAMETER EXTRACTION

By following the matrix manipultion scheme, it is possible to extract the intrinsic circuit elements. They are related to the active y parameters given above in (1)–(4). There are eight element values and eight data values (real and imaginary parts of y_{ij} at each frequency point of interest), so the circuit is fully determined. The relations are

$$C_{gs} = \frac{1}{\omega}\cdot\frac{|y_{11}+y_{12}|^2}{\mathrm{Im}(y_{11}+y_{12})} \tag{5}$$

$$R_i = \frac{1}{\omega C_{gs}}\cdot\frac{\mathrm{Re}\, y_{11}}{\mathrm{Im}(y_{11}+y_{12})} \tag{6}$$

$$C_{dc} = C_{gs}\cdot\frac{\mathrm{Re}\, y_{12}}{\mathrm{Re}\, y_{11}} \tag{7}$$

$$C_{dg} = -\frac{\mathrm{Im}\, y_{12}}{\omega} - \frac{\omega^2\tau_1\tau_2}{1+(\omega\tau_2)^2}C_{gs} \tag{8}$$

$$C_{ds} = \frac{\mathrm{Im}(y_{22})}{\omega} - C_{dg} - C_{dc}\left(1 - \frac{\omega^2\tau_1\tau_2}{1+(\omega\tau_2)^2}\right) \tag{9}$$

$$\tau = \frac{1}{\omega}\cdot\tan^{-1}\left(\frac{\mathrm{Im}(y_{12}-y_{21})}{\mathrm{Re}(y_{21}-y_{12})}\right) \tag{10}$$

$$R_{ds} = \frac{1}{\mathrm{Re}\, y_{22}}\Big|_{\omega\to 0} \tag{11}$$

$$g_m = \mathrm{Re}\, y_{21}\big|_{\omega\to 0} \tag{12}$$

TABLE II
COMPARISON OF COMPONENT ACCURACY USING MODEL I AND MODEL II

Component	Model I Accuracy	Model II Accuracy	Remarks
g_m, R_{ds}	good	good	
R_i, C_{gs}, C_{gd}	good	good	Calculations should use $[S]\|_{f>4\,\mathrm{GHz}}$
C_{ds}	poor	good	Model I overestimates this value
τ	poor	good	Unreliable value using model I (too low) Model II calculations should use $[S]\|_{f>4\,\mathrm{GHz}}$
C_{dc}	not included	good	Calculations should use $[S]\|_{f>4\,\mathrm{GHz}}$

where

$$\tau_1 = R_i C_{\mathrm{dc}}$$

$$\tau_2 = R_i(C_{gs} + C_{\mathrm{dc}}).$$

The linear transconductance, g_m, and the drain/source resistance, R_{ds}, may be expressed through the intrinsic low-frequency S parameters:

$$g_m = \frac{|S_{21}|}{Z_0(1+|S_{22}|)} \tag{13}$$

$$R_{ds} = \frac{Z_0(1+|S_{22}|)}{(1-|S_{22}|)} \tag{14}$$

where Z_0 is the characteristic impedance of the measurement system. These are the only elements, within an intrinsic FET, that have simple relationships with the measured S parameters. The other six elements characterizing the active FET are determined conveniently by using the new equations (5)–(10). Note here that it is not advisable to use S parameters at frequencies that are too low. Extensive numerical simulations have shown that measured S parameters at lowest C band (4–8 GHz) are advisable. This is due to the fact that the magnitude of S_{11} is close to unity at low frequencies.

IV. MEASUREMENTS

The S parameters of a MODFET with a mushroom gate of 0.25 μm were measured with an HP 8510 network analyzer in the frequency range 125 MHz to 25.125 GHz. The input and output contacts were probed by coplanar wafer probes (Cascade).

The complete equivalent circuit consists of CPWG's at the input and output of the FET, corresponding to the actual pattern layout. The parasitic resistances and the intrinsic element part then form the complete equivalent circuit (see Fig. 2). The CPWG was modeled as a symmetrical T network and was fit to the actual frequency response of the physical layout. The commercial CAD program TOUCHSTONE was used for the optimization (see Table I). Nomenclature for the CPWG structure follows that of the TOUCHSTONE user's manual.

Measured and modeled results are shown in Fig. 3. Modeled parameters were determined to

$$R_g = 7.7\,[\Omega] \qquad R_s = 1.0\,[\Omega] \qquad R_d = 4.2\,[\Omega]$$

$$R_i = 5.3\,[\Omega] \qquad R_{ds} = 440.3\,[\Omega] \qquad g_m = 36.4\,[\mathrm{mS}]$$

$$C_{gs} = 0.082\,[\mathrm{pF}] \qquad C_{dc} = 7.4\,[\mathrm{fF}] \qquad C_{dg} = 13.5\,[\mathrm{fF}],$$

$$C_{ds} = 12.1\,[\mathrm{fF}] \qquad \tau = 2.0\,[\mathrm{ps}].$$

V. ACCURACY CONSIDERATION

By using the two intrinsic circuits, it is advisable to compare the accuracy of the extracted parameters. Model I refers to the circuit used by Dambrine *et al.* [8]. Model II is the modified circuit. The preceding partitioning procedure of extrinsic elements is assumed. Remarks in Table II are general and are based on extensive numerical examinations.

VI. DISCUSSION AND CONCLUSION

A modified circuit characterizing the intrinsic or active part of a compound FET has been presented. A particular feedback capacitor and its associated capacitance, C_{dc}, was added to the previous circuit. Recently, Khatibzadeh and Trew [9] reported in a rigorous and powerful manner an analytic calculation of this capacitance. Here, for the first time, its relation to two-port parameters is given. In [11] and [12] it is shown that this capacitance has a significant influence on the high-frequency performance of compound FET's.

A comparison between calculated and experimental results shows the main difference in S_{12} performance [8]. This can be related to the fact that $\mathrm{Re}(y_{12}) = 0$ for model I. In model II, $\mathrm{Re}(y_{12}) \sim f^2$. Experimental results confirm this particular frequency behavior. Hence, a closer fit between modeled and experimental S_{12} is obtained. The control voltage is shifted to a series connection of $R_i - C_{gs}$. That is the Curtice convention [10]. Whether the control voltage is taken over the $R_i - C_{gs}$ combination or just C_{gs} alone has among microwave engineers been considered a minor problem. However, it was first pointed out in [13] that the different control voltage modeling resulted in different power gain characteristics at high frequencies.

When a circuit model is used to represent a transmission line, a characteristic impedance is developed which is repeated at comparable points (such as the ends of T or π sections). Here, both types of sections can accurately model the CPWG structure because it has a very short physical length compared with the wavelength. Unsymmetrical sections (inclusion of additional pad capacitors) should be considered in the general case; this is related to the physical layout of the device.

In Table II we put special emphasis on the fact that parameter extraction calculations should use measured S parameters at lowest C band (4–8 GHz). This is related to the fact that $|S_{11}| \to 1$ for low frequencies. To increase accuracy and obtain consistent values it has been found that the magnitude of S_{11} should be closer to 0.9 then to unity. This is usually the case at C band.

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D-Band Subharmonic Mixer with Silicon Planar Doped Barrier Diodes

Ulrich Güttich, Karl M. Strohm, and Friedrich Schäffler

***Abstract*—A subharmonically pumped mixer for RF frequencies in the D-band range has been realized applying silicon planar doped barrier (PDB) diodes grown by molecular beam epitaxy (MBE). Excellent RF performance data have been achieved with a finline/microstrip mixer design.**

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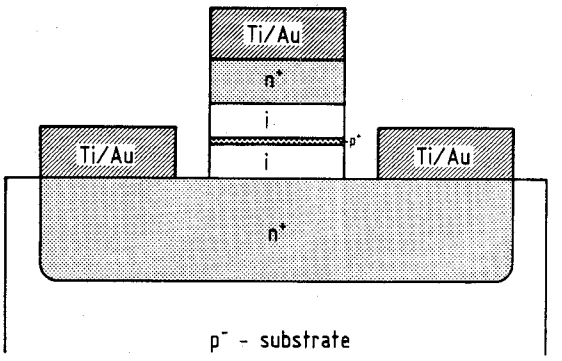

Fig. 1. Schematic cross section of PDB diode with active layer sequence and ohmic contacts.

I. Introduction

Subharmonically pumped integrated mixers (SHM's) offer many advantages over conventional down-converters, particularly at elevated RF frequencies, where local oscillator pump power and phase noise requirements are difficult to attain. SHM's realized as a finline or microstrip configuration [1], [2] have demonstrated conversion loss and noise comparable to the best fundamental balanced mixers up to 100 GHz. However, Schottky diode pairs conventionally applied in SHM's have to be matched very carefully to minimize loop inductance effects [3]. This problem can be overcome by employing planar doped barrier (PDB) diodes [4], the symmetric $I-V$ characteristic of which is an inherent property of the device and not the result of matching two separate antiparallel diodes. In addition, the required LO pump power can be reduced by lowering the barrier height of the device to a value much smaller than that of a Schottky diode. Furthermore, designing the mixer circuit is simplified since only one device, instead of two antiparallel connected diodes, is involved. The advent of molecular beam epitaxial (MBE) growth techniques now has enabled silicon PDB structures (n^+-i-p^+-i-n^+) to be grown for applications up to 140 GHz.

II. Diode Processing and DC Characteristics

The PDB diodes are fabricated on high-resistivity silicon substrates (p-type, resistivity > 3000 $\Omega \cdot$cm) in a coplanar configuration. First, oxide windows are defined and highly doped n^+ buried regions are established using an As double implantation and diffusion process (sheet resistance $< 7\ \Omega$ per square, carrier concentration $> 10^{20}$ cm^{-3}). The doping profile is realized by silicon MBE growth. The PDB is a majority carrier device structure with an extremely thin and fully depleted p^+ acceptor layer to form a triangular potential profile of predetermined shape and height. For a subharmonic mixer, a symmetric $I-V$ characteristic is required and therefore the acceptor p^+ layer has to be positioned in the center of the undoped intrinsic region (Fig. 1). The design of the doping profile is calculated using formulas reported in [5]. The epitaxial process is performed in an ATOMIKA Si-MBE machine described in detail elsewhere [6]. Growth commences with a highly n-doped (Sb, typically $> 2 \cdot 10^{18}$ cm^{-3}) buffer layer of about 20 nm thickness. The barrier structure itself consists of a p-type doping spike of 10 to 20 nm thickness between two equally wide, nominally undoped layers. Gallium evaporated from a conventional effusion cell is used as spike acceptor material. Doping by secondary implantation is employed to achieve the required doping levels and abruptness. A 0.2-μm-thick n^+ top layer used for the

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